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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,280	07/25/2006	Masato Mori	2006_1203A	4846

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EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,280	MORI ET AL.	
	Examiner	Art Unit	
	AJAY K. ARORA	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *6-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/7/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-5 and 13-16, and further within Group I, election of Embodiment 1 of Figure 1 on which claims 1-12 read (i.e. election of claim 1-5 that belong both to Group I and Embodiment 1 of Figure 1) in the reply filed on 12/01/2008 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claim 5 recites the limitation "first chip component included in said first chip components" (emphasis added) in lines 12-13. There is insufficient antecedent basis for this limitation in the claim. Prior reference is to "a first chip component" or "chip

components", and not to "first chip components" (emphasis added). For the purpose of this office action, it will be assumed that the recited limitation "first chip component included in said first chip components" is equivalent of "first chip component included in said chip components"

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by IDS reference NEC (Japanese patent JP 60-176569, which is shown as reference BA in IDS of 01/07/2009), hereinafter NEC. Note that for the above reference, the partial English translation provided with the IDS of 01/07/2009 identifies assignee as NEC IC Microcomputer System Ltd, but names of inventors have not been provided in the translation. Identification of any part of NEC reference in this office action is with respect to the above mentioned partial English translation, wherein pages 1-3 have text in English and pages 4-5 show Figures 4-9.

Regarding claim 1, NEC (refer to Figures 7 and 8 on page 5) teaches a circuit board (comprising 56) including chip components (two of 51 and one of 51') mounted thereon, the circuit

board comprising:

a substrate (56) including electrode patterns (54) formed thereon;

plural first chip components (two chip components designated 51) which are included in said chip components and mounted through a conductive bonding material (55) on said substrate (56); and

a second chip component (51') which is included in said chip components and mounted through a conductive bonding material (55) on a side of said plural first chip components (51) opposite from said substrate; wherein one first chip component and the other first chip component included in said plural first chip components have substantially a same height on said substrate (see 51 in Figure 9) , and said second chip component (51') is bonded at one electrode (52b') to an electrode (52b) of said one first chip component (51 shown on left side of Figure 9) and is bonded at the other electrode (52a') to an electrode (52a) of said other first chip component (51 shown on right side of Figure 9).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over NEC.

Regarding claim 2, NEC teaches substantially the claimed structure but does not teach that said plural first chip components and said second chip component have “lengths of 2 mm or less”. Since the applicant has not established the criticality of lengths stated and since these lengths are in common use in similar devices in the art, it would have been obvious to one of ordinary skill in the art to use these values in the device of NEC. Where patentability is said to be based upon particular chosen dimension or upon another variable recited in a claim, the applicant must show that the chosen dimensions

are critical. In re Woodruff, 919 F2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

10. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over NEC in view of Toyosawa (US 2001/0054751), hereinafter Toyosawa.

Regarding claim 3, NEC teaches substantially the claimed structure but does not teach that said plural first chip components and said second chip component are “resistors, condensers or inductors”. Toyosawa (refer to Figure 1) teaches stacking of first chip component (11) and second chip component (12), and further teaches that a chip component may be replaced by a capacitor (page 5, para 0088 and page 6, para 0091). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify NEC so that said plural first chip components and said second chip component are condensers. The ordinary artisan would have been motivated to modify NEC for at least the purpose of utilizing passive components in the circuit which may be required for impedance matching.

Regarding claim 4, NEC teaches substantially the claimed structure but does not teach “a reinforcing resin configured to cover junctions between said plural first chip components and said second chip component on said substrate". Toyosawa (refer to Figure 1) teaches stacking of first chip component (11) and second chip component (12) wherein a reinforcing resin (30) configured to cover junctions between said first chip component and said second chip component. It would have been obvious to one of

ordinary skills in the art at the time of the invention to modify NEC so that a reinforcing resin configured to cover junctions between said plural first chip components and said second chip component on said substrate is provided. The ordinary artisan would have been motivated to modify NEC for at least the purpose of protecting the devices junctions from environmental contaminants.

Regarding claim 5, NEC (refer to Figures 7 and 8 on page 5) teaches a circuit board (comprising 56) including chip components (two of 51 and one of 51') mounted thereon, the circuit board comprising:

a substrate (56) including electrode patterns (54) formed thereon;

a first chip component (51 shown to the left in Figures 8-9) which is included in said chip components and mounted through a conductive bonding material (55) on said substrate; and

a second chip component (51') which is included in said chip components and mounted through a conductive bonding material (55) on a side of said first chip components opposite from said substrate;

NEC does not disclose that first chip component included in said first chip components is "a component of a different type from the second chip component". Toyosawa (refer to Figure 1) teaches stacking of first chip component (11) and second chip component (12), and further teaches that the first chip components may be a component of a different type from the second chip component (page 5, para 0088 and page 6, para

0092). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify NEC so that said first chip components is a component of a different type from the second chip component. The ordinary artisan would have been motivated to modify NEC for at least the purpose of utilizing components with different functions that complement each other (see page 6, para 0092) wherein the stacking arrangement reduces required board area.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./
Examiner, Art Unit 2892

/Hoai v Pham/
Primary Examiner, Art Unit 2892